CLAIMS

1. A method for manufacturing a TFT array substrate in which at least (a) a gate insulating film, (b) a semiconductor layer and (c) a metal layer are sequentially formed in this order of (a), (b) and (c), and using one resist pattern formed by a photolithography, a part of the metal layer is selectively removed, to form a source line, together with the semiconductor layer beside the source line,

wherein a passivation film is formed after the formation of the source line and the removal of the semiconductor layer beside the source line, a resist pattern to selectively remove the passivation film is formed on the passivation film, and using the resist pattern, the passivation film above the source line, the passivation film beside the source line and the gate insulating film beside the source line are removed to, thereby, expose the semiconductor layer under the source line.

2. A method for manufacturing a TFT array substrate according to Claim 1, wherein a portion protruding beside the source line is removed from the exposed semiconductor layer under the source line through etching utilizing the resist pattern to selectively remove the passivation film and/or the source line as a mask.

3. A method for manufacturing a TFT array substrate according to Claim 1, wherein a portion protruding beside the source line is removed from the exposed semiconductor layer under the source line through etching utilizing the selectively removed passivation film and/or the source line as a mask.

4. A method for manufacturing a TFT array substrate in which at least (a) a gate insulating film, (b) a semiconductor layer and (c) a metal layer are sequentially formed in this order of (a), (b) and (c), and using one resist pattern formed by a photolithography, a part of the metal layer is selectively removed, to form a source line, together with the semiconductor layer beside the source line,

wherein no passivation film is formed after the formation of the source line and the removal of the semiconductor layer beside the source line.

5. A method for manufacturing a TFT array substrate in which at least (a) a gate insulating film, (b) a semiconductor layer and (c) a metal layer are sequentially formed in this order of (a), (b) and (c), and using one resist pattern formed by a photolithography, a part of the metal layer is selectively removed, to form a source line, together with the semiconductor layer beside the source line,

wherein no passivation film is formed after the formation of the source line and the removal of the semiconductor layer beside the source line, so that the source line and the semiconductor layer under the source line remain exposed, and

a portion protruding beside the source line is removed from the exposed semiconductor layer under the source line through etching utilizing the source line as a mask.

6. A method for manufacturing a TFT array substrate according to Claim 1, 2, 3, 4 or 5, wherein a ITO film is further formed, and through patterning to selectively remove the ITO film, the ITO film

on the source line is left to form the ITO film covering the source line.

7. A method for manufacturing a TFT array substrate in which at least (a) a gate insulating film, (b) a first semiconductor layer, (c) a second semiconductor layer and (d) a metal layer are sequentially formed in this order of (a), (b), (c) and (d), and a resist pattern comprising a region in which photoresist is removed, a region in which photoresist has a small thickness and a region in which photoresist has a great thickness is further formed by means of a photolithography,

wherein the metal layer, the second semiconductor layer and the first semiconductor layer are removed in the region in which photoresist is removed,

the metal layer and the second semiconductor layer are removed in the region in which photoresist has a small thickness,

and the metal layer, the second semiconductor layer and the first semiconductor layer are left remained in the region in which photoresist has a great thickness to form a source line with the metal layer left remained, and

wherein a region adjacent to the source line is the region in which photoresist has a small thickness, so that the metal layer and the second semiconductor layer are removed and the first semiconductor layer is left remained.

8. A method for manufacturing a TFT array substrate in which at least (a) a gate insulating film, (b) a first semiconductor layer, (c) a second semiconductor layer and (d) a metal layer are sequentially formed in this order of (a), (b), (c) and (d), and a resist pattern comprising

a region in which photoresist is removed, a region in which photoresist has a small thickness and a region in which photoresist has a great thickness is further formed by means of a photolithography,

wherein the metal layer, the second semiconductor layer and the first semiconductor layer are removed in the region in which photoresist is removed,

the metal layer and the second semiconductor layer are removed in the region in which photoresist has a small thickness,

and the metal layer, the second semiconductor layer and the first semiconductor layer are left remained in the region in which photoresist has a great thickness to form a source line with the metal layer left remained,

wherein a region adjacent to the source line is the region in which photoresist has a small thickness, so that the metal layer and the second semiconductor layer are removed and the first semiconductor layer is left remained, and

wherein a passivation film is formed aftre removal of the photoresist, a resist pattern to selectively remove the passivation film is formed on the passivation film, and using the resist pattern, the passivation film above the source line and the passivation film beside the source line are removed to, thereby, expose the second and first semiconductor layers under the source line.

9. A method for manufacturing a TFT array substrate according to Claim 8, wherein a portion protruding beside the source line is removed from the exposed second and first semiconductor layers under the source line through etching utilizing the resist pattern to

selectively remove the passivation film and/or the source line as a mask.

10. A method for manufacturing a TFT array substrate according to Claim 8, wherein a portion protruding beside the source line is removed from the exposed second and first semiconductor layers under the source line through etching utilizing the selectively removed passivation film and/or the source line as a mask.

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11. A method for manufacturing a TFT array substrate in which at least (a) a gate insulating film, (b) a first semiconductor layer, (c) a second semiconductor layer and (d) a metal layer are sequentially formed in this order of (a), (b), (c) and (d), and a resist pattern comprising a region in which photoresist is removed, a region in which photoresist has a small thickness and a region in which photoresist has a great thickness is further formed by means of a photolithography,

wherein the metal layer, the second semiconductor layer and the first semiconductor layer are removed in the region in which photoresist is removed,

the metal layer and the second semiconductor layer are removed in the region in which photoresist has a small thickness,

and the metal layer, the second semiconductor layer and the first semiconductor layer are left remained in the region in which photoresist has a great thickness to form a source line with the metal layer left remained,

wherein a region adjacent to the source line is the region in which photoresist has a small thickness, so that the metal layer and the second semiconductor layer are removed and the first semiconductor

layer is left remained, and

wherein no passivation film is formed after removal of the resist pattern.

12. A method for manufacturing a TFT array substrate in which at least (a) a gate insulating film, (b) a first semiconductor layer, (c) a second semiconductor layer and (d) a metal layer are sequentially formed in this order of (a), (b), (c) and (d), and a resist pattern comprising a region in which photoresist is removed, a region in which photoresist has a small thickness and a region in which photoresist has a great thickness is further formed by means of a photolithography,

wherein the metal layer, the second semiconductor layer and the first semiconductor layer are removed in the region in which photoresist is removed,

the metal layer and the second semiconductor layer are removed in the region in which photoresist has a small thickness,

and the metal layer, the second semiconductor layer and the first semiconductor layer are left remained in the region in which photoresist has a great thickness to form a source line with the metal layer left remained,

wherein a region adjacent to the source line is the region in which photoresist has a small thickness, so that the metal layer and the second semiconductor layer are removed and the first semiconductor layer is left remained, and

wherein no passivation film is formed after removal of the resist pattern, and a portion protruding beside the source line is removed from the second and first semiconductor layers under the

source line through etching utilizing the source line as a mask.

13. A method for manufacturing a TFT array substrate according to Claim 7, 8, 9, 10, 11 or 12, wherein a ITO film is further formed, and through patterning to selectively remove the ITO film, the ITO film on the source line is left to form the ITO film covering the source line.

14. A method for manufacturing a TFT array substrate according to Claim 12, wherein a photoresist on a lower electrode pad at the end of the gate line is removed through a peripheral exposing step in which no mask is used, so that a part of the gate insulating film is removed by etching to expose the lower electrode pad at the end of the gate line.